REMARKS

Reconsideration of the application is requested.

Applicant acknowledges the Examiner's confirmation of receipt of applicant's certified copy of the priority document for the German Patent Application 198 36 956.5, filed August 14, 1998 supporting the claim for priority under 35 U.S.C. § 119 and applicant's certified copy of the priority document for the International Patent Application PCT\DE99\02388, filed August 2, 1999 supporting the claim for priority under 35 U.S.C. § 119.

Claims 1 and 5-16 are in the application. Claims 1 and 5 have been amended. *Claims 2-4 have been canceled to facilitate prosecution of the instant application.*

In "Claim Rejections - 35 USC § 102" item 5 on page 2 of the above-identified Office Action, claims 1-3, 11-12, and 14-15 have been rejected as being fully anticipated by U.S. Patent No. 5,943,613 to *Wendelrup, et al.* (hereinafter **WENDELRUP**) under 35 U.S.C. § 102(e).

In "Claim Rejections - 35 USC § 103" item 25 on page 6 of the above-identified Office Action, claim 13 have been rejected as being obvious over **WENDELRUP** under 35 U.S.C. § 103(a).

In "Claim Rejections - 35 USC § 103" item 13 on page 4 and item 27 on page 6 of the above-identified Office Action, claims 4-10 and 16 have been rejected as being obvious over **WENDELRUP** in view of U.S. Patent No. 5,560,024 to *Harper, et al.* (hereinafter **HARPER**) under 35 U.S.C. § 103(a).

The rejection has been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found in claims 2-4 and on pages 7 and 9-11 of the specification of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a method for supplying a clock signal to processor-controlled apparatuses including:

> generating a quartz frequency with a clock quartz;
>
> providing a clock frequency based on the quartz frequency of the clock quartz to a device for determining a clock time;
>
> **providing the clock frequency to a processor device** during operational time periods of low processor load or no processor load and otherwise providing a different clock frequency to the processor device;
>
> switching the processor device to **a clockless state** during operational time periods **with no processor load;** and

selecting the clock signal as a function of processor load according to the following:

during operational time periods with low processor load or **no processor load**, providing **the same clock signal** to **the processor device** as to **the device for determining a clock time**, and

during operational time periods with processor loading, providing a clock signal based on a system clock to the processor device.

Claim 11 calls for, *inter alia*, a configuration for supplying a clock signal to processor-controlled apparatuses including:

a clock selector unit connected to the processor device for **selecting a frequency** to be fed to the processor device, **as a function of a processor load;**

an oscillator having a clock quartz for generating a quartz frequency, the oscillator being configured to feed a clock frequency based on the quartz frequency or a frequency derived therefrom to the device for determining the clock time;

said clock selector unit feeding a clock frequency based on the quartz frequency or on a frequency derived therefrom to the processor device when there is no processor load or when there is low processor load; and

otherwise the processor device being clocked with a system clock.

Claim 12 calls for, *inter alia*, a method for conserving power of a processor device of a processor-controlled apparatus operating by a clock supply system driven according to a usage factor including:

generating a quartz frequency as a function of a quartz clock;

providing the quartz frequency to a real-time clock;

selecting a clock frequency as a function of processor load;

generating a clock signal based on the selected clock frequency; and

providing the generated clock signal to the processor device.

The **WENDELRUP** reference discloses a method and apparatus for reducing power consumption in a communication device. In a standby mode described in **WENDELRUP**, a high power clock is powered down and a lower power, low frequency clock is used to maintain system synchronization. More specifically, **WENDELRUP** states "a mobile phone may also have a simple low-power real time clock (RTC) for showing time on a communications device display. This clock typically runs at a much lower frequency (32.768 kHz) and is typically not very accurate (e.g., 10-20 ppm, depending upon the quality of the clock crystal)" (col. 1, lines 28-33). **WENDELRUP** also indicates that the described system uses "a low power, low frequency real time clock (RTC) oscillator and synchronization means for synchronizing the RTC oscillator to a relatively higher power and higher frequency master clock." And that "During a standby or idle mode, the high frequency master clock is powered down, and system timing is maintained by the lower frequency clock." (Col. 2, lines 24-30).

WENDELRUP also indicates that the device operates in two modes, "a normal operation mode and a standby operation mode"

(Col. 3, lines 4-5). The normal operation mode of **WENDELRUP** uses a reference clock and the standby operation mode of **WENDELRUP** uses a separate standby clock operating at a lower frequency than the reference clock. However, contrary to the assertions of the above-identified Office Action, **WENDELRUP** does not teach or suggest that the either the normal operation mode or the standby operation mode are selected based on the processor load as indicated in claims 11 and 12 of the instant application.

Mere designation of "standby mode" in **WENDELRUP** does not indicate that the standby operation mode of **WENDELRUP** is equivalent to "operational time periods with low processor load or no processor load", as recited in claim 1 of the instant application. In Fact, **WENDELRUP** states, "During standby mode, the equipment is active only during short intervals when listening for a page, and is powered down during the remaining intervals." As such, standby mode is more likely a power conservation mode imposed on the system and not dictated by processor load. Moreover, there is no indication that either the normal mode or standby mode of **WENDELRUP** provide "the same clock signal to the processor device as to the device for determining a clock time" as recited in claim 1 of the instant application.

Nor does **WENDELRUP** indicate that the processor can **switch to a clockless state** when there is no processor load. Moreover, contrary to the assertions found in the above-identified Office Action, there is no indication that during low or no load operational time periods that the same clock signal is provided to both the processor device and the device for determining the clock time.

Clearly, **WENDELRUP** does not show "**selecting a frequency** to be fed to the processor device, **as a function of a processor load**" as recited in claim 11 of the instant application, nor does **WENDELRUP** teach or suggest "**selecting a clock frequency as a function of processor load**" as recited in claim 12 of the instant application. **WENDELRUP** does not show "**switching the processor device to a clockless state** during operational time periods with no processor load" as recited in claim 1 of the instant application. Nor does **WENDELRUP** teach or suggest "providing **the same clock signal** to **the processor device** as to **the device for determining a clock time**" during low or no processor loading operational time periods as recited in claim 1 of the instant application.

The **HARPER** reference discloses a computer power management system that powers down various sections of a computer that are not being used. More specifically, as indicated in the

above-identified Office Action, **HARPER** states, "The state controller **stops** the main system oscillator upon receipt of a so-called sleep request signal. This request signal comes from a bit in a particular register accessible to the microprocessor of the computer. When this bit is set, the microprocessor "clock" is **stopped** on the next falling edge of the main system clock signal." (Col. 4, lines 38-43, emphasis added). However, "stopping" a clock as described in **HARPER** is clearly not "switching the processor device to a clockless state" as recited in claim 1 of the instant application. In further contrast to **HARPER** where the clock is "**stopped**", claim 1 of the instant case indicates that during periods of no processor load, "the same clock signal" is provided to both the processor device and the device for determining the clock time.

Clearly, the proposed combination of **WENDELRUP** and **HARPER** do not show "**switching the processor device to a clockless state** during operational time periods with no processor load" as recited in claim 1 of the instant application. Nor do **WENDELRUP** and **HARPER** teach or suggest "providing **the same clock signal** to **the processor device** as to **the device for determining a clock time**" during low or no processor loading operational time periods as recited in claim 1 of the instant application. Furthermore, the proposed combination of **HARPER**

and **WENDELRUP** do not show "**selecting a frequency** to be fed to the processor device, **as a function of a processor load**" as recited in claim 11 of the instant application, nor do **HARPER** and **WENDELRUP** teach or suggest "**selecting a clock frequency as a function of processor load**" as recited in claim 12 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1, 11, and 12. Claims 1, 11, and 12 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1 or claim 12.

In view of the foregoing, reconsideration and allowance of claims 1 and 5-16 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith

should be charged to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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